

10792087

**Amendments to the Specification**

Kindly amend the specification as follows:

Page 1, between the title and the heading "**BACKGROUND OF THE INVENTION**", insert

**--CROSS REFERENCE TO RELATED APPLICATIONS**

This is a divisional application of application Serial No. 10/073,022, filed March 1, 2004, which is hereby incorporated by reference in its entirety for all purposes.—  
*is now abandoned*  
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***Please replace the paragraph beginning on page 5, line 20 with the following amended paragraph:***

In this level shift circuit, the output of the inverter 1215 is at high level when the input signal IN is at low level. Therefore the nMOS transistor 1213 is OFF, and the nMOS transistor 1214 is ON. Since the nMOS transistor 1214 is ON, the potential of the node N2, that is, the signal level of the output signal OUT, is at low level. As a result, the pMOS transistor 1211 is ON, therefore the potential of the node ~~[[N2]]~~ N1 is at high level. This means that the pMOS transistor 1212 is OFF.

***Please amend the abstract as follows:***

A level shift circuit ~~whereby a voltage shift amount is large, operation speed is fast, and the power consumption is low.~~ A ~~p-type~~ including a first transistor ~~[[is]]~~ circuit connected between ~~[[the]]~~ a power supply line and ~~[[the]]~~ a first node, a ~~p-type~~ second